IN THE DETAILED DESCRIPTION

Replace paragraph [0010] with the following:

[0010] FIG. 1 is a flowchart of an interrupt handler 100 according to one embodiment of the invention. In a translation lookaside buffer (TLB) miss, an interrupt occurs because a block of data to be accessed is not present in the hardware TLB registers. In response, an interrupt handler is initiated at 105, and the virtual address needing to be resolved is read from the hardware register. In one embodiment, a memory block size is approximately 4K bytes. Bits 20-31 of the virtual address are used to index into a base dispatch decode table at 110. At 115, a level 1 decode table is read to obtain a base offset into a level 2 decode table. The level 1 decode table entry plus bits 16-20 of the virtual address are used to obtain the offset into the level 2 decode table at 120. In one embodiment, a single half-word in the second level table corresponds to two hardware register words. The single half-word may be formed to minimize operations of a computer implementing the method. In a further embodiment, a single half-word in the second level table corresponds to two hardware register words for all memory pages in the block.

Replace paragraph [0011] with the following:

[0011] At 125, the level 2 decode table entry of 32 bits is read. It is either an offset to a level 3 decode table, or data for processing the current block. Bits 12-15 are used at 130 to index into a 16 bit valid array of the level 2 entry. If the selected bit is 0, then a further level 3 decoding is performed at 145. Otherwise, this is a valid block for level 2 decoding, and the virtual address is concatenated 135 with the remaining 16 bits of the level 2 decode table entry and a Process ID to fill the TLB miss control hardware registers. The least significant bits of the virtual address and the real address are the same. In one embodiment, a single half-word in the second level table corresponds to two hardware register words and a single word in the level three table corresponds to two hardware register words.